

# Jia Shuo Tom Yue

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416.560.8913

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- AT A GLANCE**
- » Enthusiastic, hard-working individual
  - » Quick learner of electrical and computer engineering concepts and methods

**TECHNICAL**      **General**

- SKILLS**
- » Fluent with all major Windows releases and \*nix
  - » Familiar with all major productivity suites, Adobe CS
  - » Fluent with XHTML/CSS, XML, LaTeX
  - » Typical typing speed 120 wpm

**Computer Science / Computer Engineering**

- » Fluent in C++; experience in sockets / multithread programming
- » Competent in PHP, Perl, Java; Can use MySQL with effort
- » Experience with low-level debugging tools such as `gdb`, `gprof`, `Valgrind`

**Digital Electronics / Reconfigurable Hardware / FPGA**

- » Familiar with FPGA synthesis, placing and routing flow
- » Familiar with Xilinx EDK and various IPs

**WORK**                      **VSLI Research Group, University of Toronto**                      **April – August 2006**

**EXPERIENCE**              **Supervisor: Professor Paul Chow, ECE**

- » Renewed ECE532 Digital Hardware's laboratory curriculum
- » Investigated the impact on placing and routing of a network-on-chip topology on a FPGA fabric as a result of increased consumption of physical resources:
  - Wrote program to automatically convert topology descriptions into Xilinx EDK project files
  - Wrote scripts to synthesize, place, route and report projects
  - Collected and analysed data
  - Co-authored paper reporting findings (see **PUBLICATIONS** below)
  - Created poster and presented at faculty-wide research conferences

**ViewGenie Group, University of Toronto**                      **February – August 2006**

**Supervisor: Professor Parham Aarabi, ECE**

- » Designed and implemented the login system for *ViewGenie*, an image storage and retrieval network
- » Interfaced with database and AJAX applications

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<b>WORK</b>	<b>iQua Research Group, University of Toronto</b>	<b>April – August 2005</b>
<b>EXPERIENCE</b>	<b>Supervisor: Professor Baochun Li, ECE</b>	
<b>(CONT'D)</b>	» Co-implemented <i>iOverlay</i> , a message engine for overlay network applications	
	» Optimised engine to achieve >600% performance increase over earlier versions	
	» Implemented algorithms, test scripts and batch files	
	» Documented design and implementation process	
	» Presented project at faculty-wide Undergraduate Research Day 2005	
<b>ACADEMIC</b>	» Recipient of Governor General's Academic Medal	
<b>ACHIEVEMENTS</b>	» Consistently ranks within top 8 in the Engineering Science program (0T8)	
	» Recipient of numerous entrance and in-course scholarships	
	» Recipient of Engineering Science Research Opportunity Grant (summer 2005)	
	» Recipient of NSERC Undergraduate Summer Research Award (summer 2006)	
<b>PUBLICATIONS</b>	» M. Saldaña, L. Shannon, J. S. Yue, S. Bian, J. Craig and P. Chow, "Routability Prediction of Network Topologies in FPGAs," submitted for review at <i>IEEE. Trans. VLSI Syst.</i>	
<b>REFERENCES</b>	available upon request	